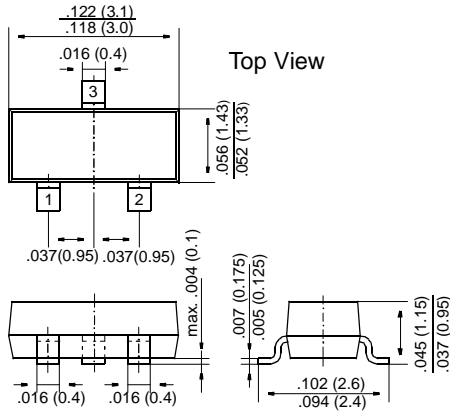


2N7002

DMOS Transistors (N-Channel)

SOT-23



Dimensions in inches and (millimeters)

Pin configuration

1 = Gate, 2 = Source, 3 = Drain

FEATURES

- ◆ High input impedance
- ◆ High-speed switching
- ◆ No minority carrier storage time
- ◆ CMOS logic compatible input
- ◆ No minority carrier storage time
- ◆ CMOS logic compatible input
- ◆ No thermal runaway
- ◆ No secondary breakdown



MECHANICAL DATA

Case: SOT-23 Plastic Package

Weight: approx. 0.008 g

Marking

S72

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Ratings at 25 °C ambient temperature unless otherwise specified

	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	60	V
Drain-Gate Voltage	V_{DGS}	60	V
Gate-Source-Voltage (pulsed)	V_{GS}	± 20	V
Drain Current (continuous)	I_D	250	mA
Power Dissipation at $T_C = 50\text{ }^\circ\text{C}$	P_{tot}	0.310 ¹⁾	W
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature Range	T_S	-55 to +150	$^\circ\text{C}$

¹⁾ Ceramic Substrate 0.7mm; 2.5 cm² area.

Inverse Diode

	Symbol	Value	Unit
Max. Forward Current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	I_F	0.3	A
Forward Voltage Drop (typ.) at $V_{GS} = 0$, $I_F = 0.3\text{ A}$, $T_j = 25\text{ }^\circ\text{C}$	V_F	0.85	V

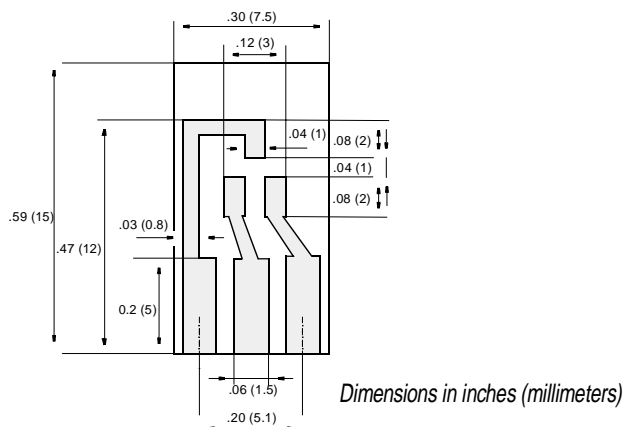
2N7002

ELECTRICAL CHARACTERISTICS

Ratings at 25 °C ambient temperature unless otherwise specified

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $I_D = 100\ \mu\text{A}$, $V_{GS} = 0$	$V_{(BR)DSS}$	60	90	—	V
Gate Threshold Voltage at $V_{GS} = V_{DS}$, $I_D = 1\ \text{mA}$	$V_{GS(th)}$	—	2	2.5	V
Gate-Body Leakage Current at $V_{GS} = 15\ \text{V}$, $V_{DS} = 0$	I_{GSS}	—	—	10	nA
Drain Cutoff Current at $V_{DS} = 25\ \text{V}$, $V_{GS} = 0$	I_{DSS}	—	—	0.5	μA
Drain-Source ON Resistance at $V_{GS} = 10\ \text{V}$, $I_D = 500\ \text{mA}$	$r_{DS(ON)}$	—	5	7.5	Ω
Thermal Resistance Junction to Substrate Backside	R_{thSB}	—	—	320 ¹⁾	K/W
Thermal Resistance Junction to Ambient Air	R_{thJA}	—	—	450 ¹⁾	K/W
Forward Transconductance at $V_{DS} = 10\ \text{V}$, $I_D = 200\ \text{mA}$, $f = 1\ \text{MHz}$	g_m	—	200	—	mS
Input Capacitance at $V_{DS} = 10\ \text{V}$, $V_{GS} = 0$, $f = 1\ \text{MHz}$	C_{iss}	—	60	—	pF
Switching Times at $V_{GS} = 10\ \text{V}$, $V_{DS} = 10\ \text{V}$, $R_D = 100\ \Omega$					
Turn-On Time	t_{on}	—	5	—	ns
Turn-Off Time	t_{off}	—	25	—	ns

¹⁾ Device on fiberglass substrate, see layout



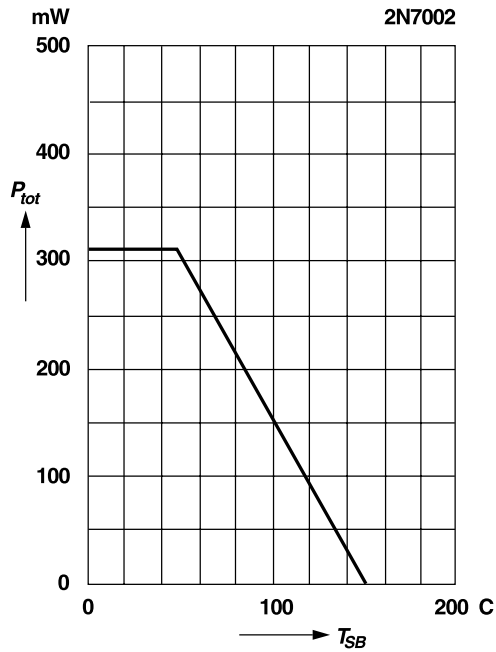
Layout for R_{thJA} test

Thickness: Fiberglass 0.059 in (1.5 mm)
Copper leads 0.012 in (0.3 mm)

RATINGS AND CHARACTERISTIC CURVES 2N7002

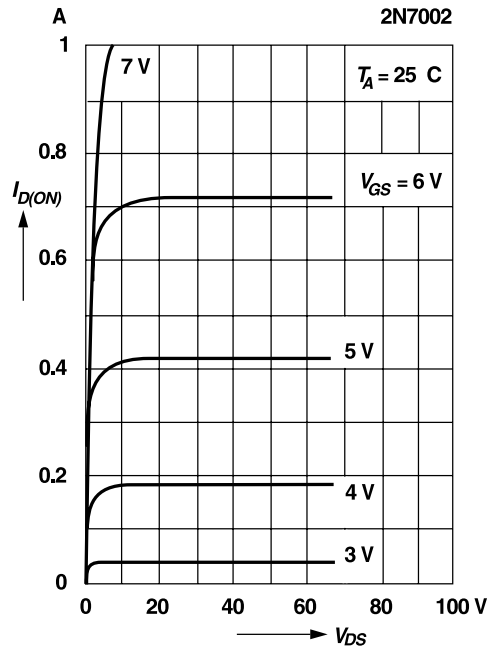
Admissible power dissipation versus temperature of substrate backside

Device on fiberglass substrate, see layout



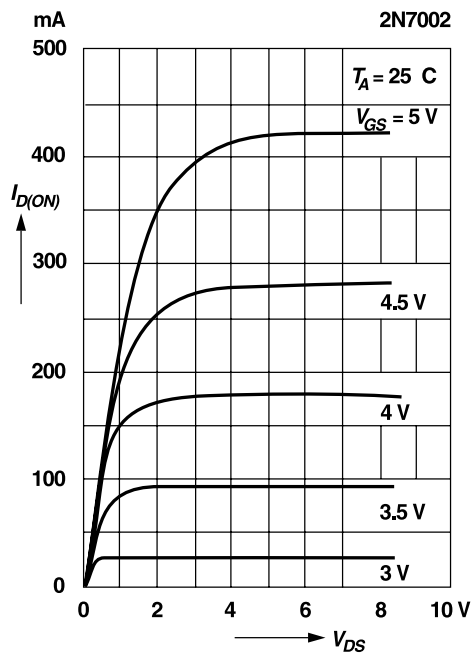
Output characteristics

Pulse test width 80 ms; pulse duty factor 1%.

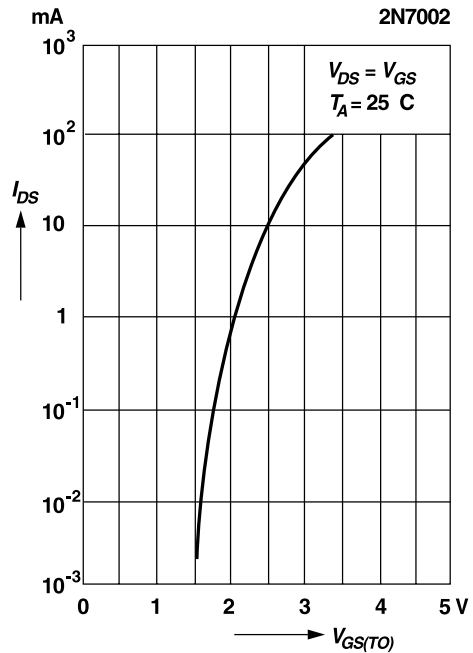


Saturation characteristics

Pulse test width 80 ms; pulse duty factor 1%.



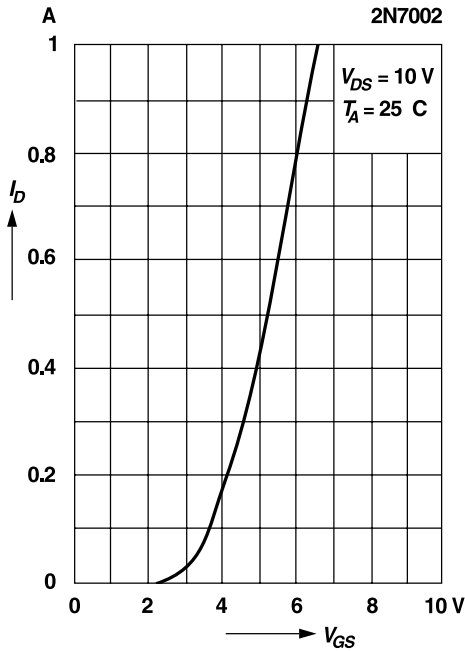
Drain-source current versus gate threshold voltage



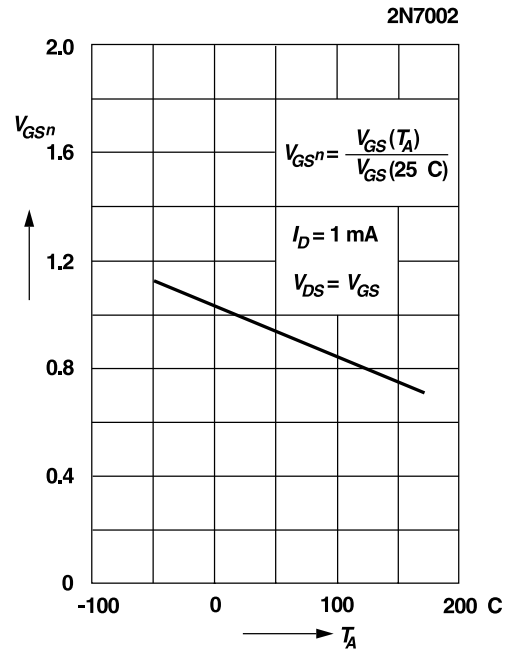
RATINGS AND CHARACTERISTIC CURVES 2N7002

**Drain current
versus gate-source voltage**

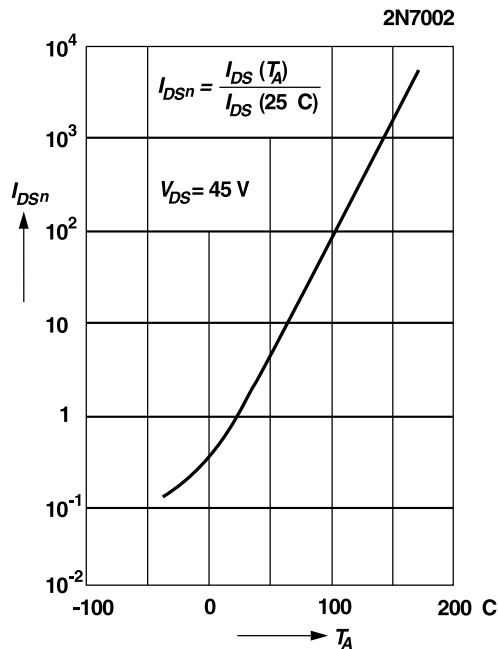
Pulse test width 80 ms; pulse duty factor 1%.



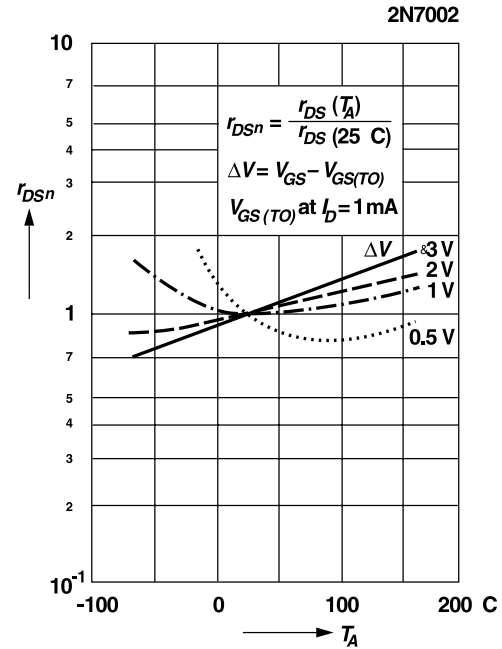
**Normalized gate-source voltage
versus temperature**



**Normalized drain-source current
versus temperature**

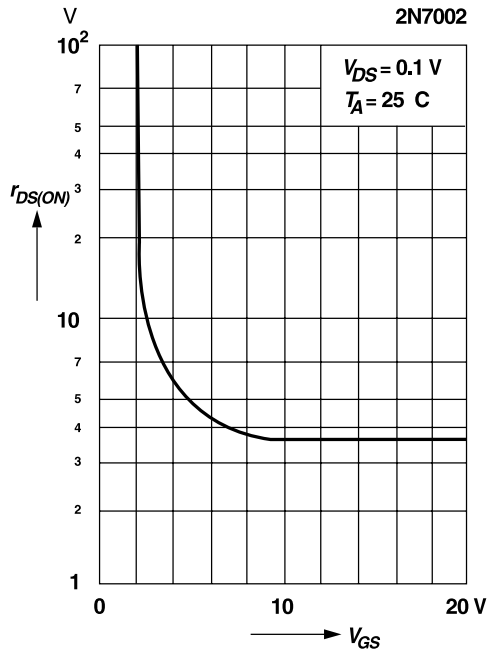


**Normalized drain-source resistance
versus temperature**



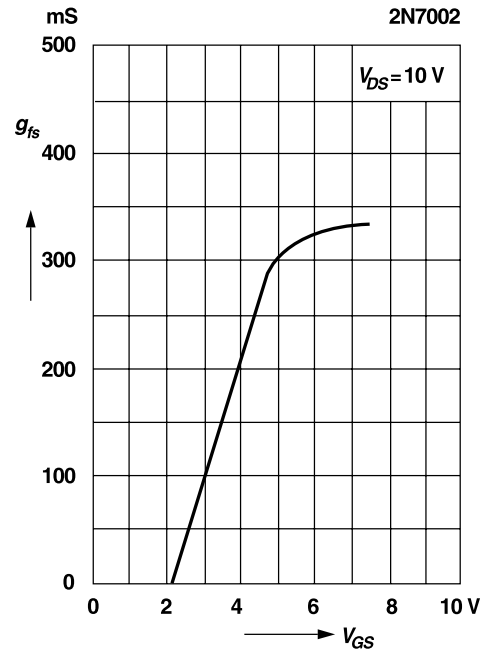
RATINGS AND CHARACTERISTIC CURVES 2N7002

**Drain-source resistance
versus gate-source voltage**



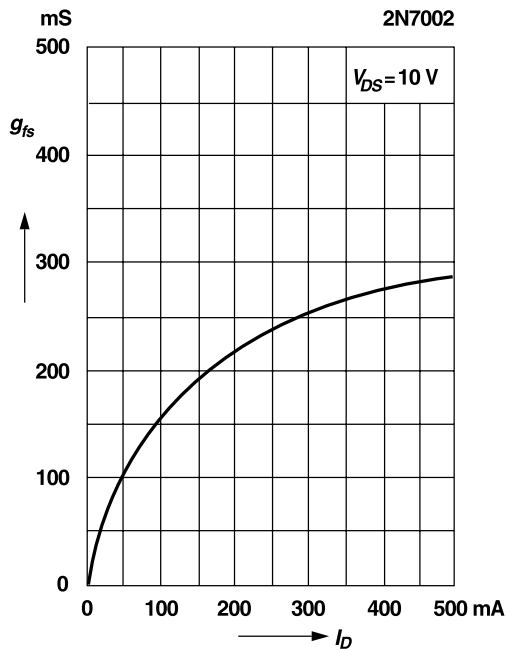
**Transconductance
versus gate-source voltage**

Pulse test width 80 ms; pulse duty factor 1%



**Transconductance
versus drain current**

Pulse test width 80 ms; pulse duty factor 1%



**Capacitance
versus drain-source voltage**

